Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the present application.

Listing of Claims:

Claims 1-49 (canceled).

50. (new) A method of synchronizing an output signal with a first clock signal, said method comprising:

producing a first timing signal based on phase-locking a first edge of the output signal to a first edge of the first clock signal;

producing a second timing signal based on a duty cycle of a delayed first clock signal; and

using the first and second timing signals to output the output signal synchronized with the first clock signal, wherein the output signal has a substantially symmetrical duty cycle.

51. (new) The method of claim 50, wherein said output signal is a data output signal.

52. (new) The method of claim 50, wherein said output signal is a timing signal.

53. (new) The method of claim 50, wherein said output signal is output by generating a rising edge of the output signal in response to the first timing signal and generating a falling edge of the output signal in response to the second timing signal.

54. (new) The method of claim 50, wherein said output signal is output by generating a rising edge of the output signal in response to the second timing signal and generating a falling edge of the output signal in response to the first timing signal.

55. (new) The method of claim 50, further comprising:

comparing a signal representative of the output signal with a local clock signal derived from the first clock signal; and

generating the delayed clock signal in response to a phase difference between the local clock signal and the signal representative of the output signal.

56. (new) The method of claim 55 further comprising:

comparing the delayed clock signal with an inverse of the delayed clock signal; and

adjusting the relative timing of the second timing signal according to a difference between a high time of the delayed clock signal and a high time of the inverse of said delayed clock signal.

57. (new) The method of claim 55 further comprising:

comparing the delayed clock signal with an inverse of the delayed clock signal; and

adjusting the relative timing of the second timing signal according to a difference between a low time of the delayed clock signal and a low time of the inverse of the delayed clock signal.

58. (new) The method of claim 57, wherein the second timing signal is generated from at least the inverse of the delayed clock signal that is adjusted to produce substantially equal time durations between occurrence of said first and second timing signals.

59. (new) The method of claim 50, wherein said output signal is a strobe signal.

60. (new) A circuit for synchronizing a first clock signal with an output signal, said circuit comprising:

means for producing a first timing signal based on phase-locking a first edge of the output signal to a first edge of the first clock signal;

means for producing a second timing signal based on a duty cycle of a delayed first clock signal; and

means for using the first and second timing signals to output the output signal synchronized with the first clock signal.

61. (new) The circuit of claim 60, wherein said output signal is a data output signal.

62. (new) The circuit of claim 60, wherein said output signal is a timing signal.

63. (new) The method of claim 60, wherein said output signal is a strobe signal.

64. (new) The circuit of claim 60, wherein said output signal is output by generating a rising edge of the output signal in response to the first timing signal and generating a falling edge of the output signal in response to the second timing signal.

65. (new) The circuit of claim 60, wherein said output signal is output by generating a rising edge of the output signal in response to the second timing signal and generating a falling edge of the output signal in response to the first timing signal.

66. (new) The circuit of claim 60, further comprising:

means for comparing a signal representative of the output signal with a local clock signal derived from the first clock signal; and

means for generating the delayed clock signal in response to a phase difference between the local clock signal and the signal representative of the output signal.

67. (new) The circuit of claim 66 further comprising:

means for comparing the delayed clock signal with an inverse of the delayed clock signal; and

means for adjusting the relative timing of the second timing signal according to a difference between a high time of the delayed clock signal and a high time of the inverse of said delayed clock signal.

68. (new) The circuit of claim 66 further comprising:

means for comparing the delayed clock signal with an inverse of the delayed clock signal; and

means for adjusting the relative timing of the second timing signal according to a difference between a low time of the delayed clock signal and a low time of the inverse of the delayed clock signal.

69. (new) The circuit of claim 68, wherein the second timing signal is generated from at least the inverse of the delayed clock signal that is adjusted to produce substantially equal time durations between occurrence of said first and second timing signals.

70. (new) The circuit of claim 60, wherein the output signal has a substantially symmetrical duty cycle.

71. (new) A memory circuit comprising:

a controller; and

a synchronizing circuit comprising:

at least one logic circuit configured to produce a delayed clock signal from a local clock signal derived from a first clock signal, and configured to produce at least first and second timing signals each associated with one of a rising and falling edge of said delayed clock signal; and

first circuitry coupled to said at least one logic circuit, configured to adjust a relative timing of at least one of said first and second timing signals to produce

substantially equal time durations between occurrence of said first and second timing signals, and configured to generate an output signal having a rising edge synchronized with a rising edge of said first clock signal in response to at least said first and second timing signals.

72. (new) The circuit of claim 71, wherein said output signal has a substantially symmetric duty cycle.

73. (new) The circuit of claim 71, wherein said at least one logic circuit includes a phase detector that detects a difference in phase between said local clock signal derived from said first clock signal and a signal representative of said output signal.

74. (new) The circuit of claim 71, wherein said first circuitry includes a comparator that measures a difference between a low time of said delayed clock signal and a low time of an inverse of said delayed clock signal.

75. (new) The circuit of claim 71, wherein said circuitry includes a comparator that measures a difference between a high time of said delayed clock signal and a high time of an inverse of said delayed clock signal.

76. (new) The circuit of claim 75, wherein said circuitry includes an arbiter that generates at least two adjustment signals from an error signal output of said comparator, said adjustment signals being used to produce at least one of said first and second timing signals.

77. (new) The circuit of claim 71, wherein at least one of said circuitry and said at least one logic circuit includes a fixed delay circuit that delays said delayed clock

signal by a fixed number of delays and a variable delay circuit that delays said second timing signal by a variable number of delays.

78. (new) A memory circuit comprising:

a controller; and

a synchronizing circuit comprising:

a first logic circuit configured to produce a delayed clock signal from a local clock signal derived from a first clock signal;

a second logic circuit configured to compare a first delay characteristic associated with said delayed clock signal with a second delay characteristic associated with an inverse of said delayed clock signal;

a third logic circuit configured to generate a first one-shot timing signal at least from said delayed clock signal and a second one-shot timing signal at least from an adjustably delayed signal associated with said inverse of said delayed clock signal;

circuitry coupled to at least said third logic circuit that adjusts said adjustably delayed signal to produce substantially equal time durations between occurrence of said first and second one-shot timing signals;

a fourth logic circuit configured to produce an output signal from at least said first and second one-shot timing signals, said output signal having a substantially symmetric duty cycle.